G1 H1 cont'd a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

40. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

J1 G2 a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring, a first diode of the plurality of first diodes including:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

G3 J1 45. (Twice Amended) The chip of claim 15 wherein the ESD positive lines are never directly connected to a steady voltage source.

51. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

52. (Amended) The chip of claim 51 wherein the switches block a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a second rate that is different from the first rate.

53. (Amended) The chip of claim 51 wherein the second diodes are forward biased when the voltage on the positive line rises at the second rate.

Please add the following new claims:

--57. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that only one second diode is connected between a pad and a positive line.

58. The semiconductor chip of claim 57 wherein a first diode of the plurality of first diodes comprises:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region.

59. The semiconductor chip of claim 58 wherein the second region is formed in the substrate, the second region and the substrate having opposite conductivity types.

60. The semiconductor chip of claim 57 wherein the ESD switches are not directly connected to a pad.

61. The semiconductor chip of claim 57 wherein none of the positive lines encircles the periphery of the chip.

62. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring:

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and

a plurality of second diodes connected to the pads so that only one second diode is connected between a pad and a positive line.

63. The semiconductor chip of claim 62 wherein a first diode of the plurality of first diodes comprises:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region.

64. The semiconductor chip of claim 63 wherein the second region is formed in the substrate, the second region and the substrate having opposite conductivity types.

65. The semiconductor chip of claim 62 wherein the ESD switches are not directly connected to a pad.

66. The semiconductor chip of claim 62 wherein none of the positive lines encircles the periphery of the chip.--